I claim:

1. A method of reducing differential-heating signal errors along a differential signal path, the method comprising the steps of:

coupling first and second transistors to different sides of said differential signal path; and

providing a differential correction signal to said differential signal path in differential response to a differential error signal generated by like terminals of said first and second transistors.

2. The method of claim 1, further including the step of establishing respective bias parameters for at least one set of same terminals of said first and second transistors that differ from said like terminals.

3. The method of claim 2, wherein said first and second transistors are bipolar junction transistors, said like terminals are emitters, same terminals of one set are collectors and their respective bias parameter is current, and same terminals of another set are bases and their respective bias parameter is voltage.

4. The method of claim 2, wherein said first and second transistors are metal-oxide semiconductor transistors, said like terminals are sources, same terminals of one set are drains and their respective bias parameter is current, and same terminals of another set are gates and their respective bias parameter is voltage.

5. The method of claim 1, wherein said providing step includes the step of amplifying said differential error signal to realize said differential correction signal.

6. The method of claim 1, wherein said differential correction signal is a differential current signal.

7. The method of claim 1, wherein said first and second transistors are coupled to one of upstream and downstream portions of said

differential signal path and said differential correction signal is provided to the other of said upstream and downstream portions.

8. The method of claim 1, wherein said coupling step includes the step of directly connecting said first and second transistors to said different sides of said differential signal path.

9. A correction sensor for reduction of differential-heating signal errors along a differential signal path, the sensor comprising:

first and second transistors coupled to different sides of said differential signal path; and

a differential error amplifier that couples a differential correction signal to said differential signal path in differential response to a differential error signal generated by like terminals of said first and second transistors.

10. The sensor of claim 9, further including a bias generator which biases at least one set of same terminals of said first and second transistors that differ from said like terminals.

11. The sensor of claim 10, wherein:

said first and second transistors are bipolar junction transistors and said like terminals are emitters;

same terminals of one set are collectors and a respective bias generator is at least one current source; and

same terminals of another set are bases and a respective bias generator is a voltage source.

12. The sensor of claim 10, wherein:

said first and second transistors are metal-oxide semiconductor transistors and said like terminals are sources;

same terminals of one set are drains and a respective bias generator is at least one current source; and

same terminals of another set are gates and a respective bias generator is a voltage source.

13. The sensor of claim 9, wherein said differential error amplifier includes a differential pair of transistors and said differential correction signal is a differential current.

14. The sensor of claim 9, wherein said first and second transistors are coupled to one of upstream and downstream portions of said differential signal path and said differential correction signal is coupled to the other of said upstream and downstream portions.

15. The sensor of claim 9, wherein said first and second transistors are directly connected to said different sides of said differential signal path.

16. An amplifier, comprising:

a differential amplifier that processes a differential signal along a differential signal path; and

a correction sensor that has first and second transistors coupled to different sides of said differential signal path and a differential error amplifier that couples a differential correction signal to said differential signal path in differential response to a differential error signal generated by like terminals of said first and second transistors;

differential-heating signal errors of said differential amplifier thereby reduced by said sensor.

17. The amplifier of claim 16, further including a bias generator that establishes respective bias parameters for at least one set of same terminals of said first and second transistors that differ from said like terminals.

18. The amplifier of claim 17, wherein said bias generator comprises first and second current sources that couple first and second currents through said first and second transistors.

19. The amplifier of claim 16, wherein said first and second transistors are bipolar junction transistors and said like terminals are

emitters of said bipolar junction transistors.

20. The amplifier of claim 16, wherein said first and second transistors are metal-oxide semiconductor transistors and said like terminals are sources of said metal-oxide semiconductor transistors.

21. The amplifier of claim 16, wherein:
said differential amplifier includes a differential pair of transistors and first and second buffers that have buffer output terminals and also have buffer input terminals coupled to differential output terminals of said differential pair;
said first and second transistors are coupled to said buffer output terminals; and
said correction sensor is coupled to said buffer input terminals.

22. The amplifier of claim 16, wherein:
said differential amplifier includes a differential pair of transistors and first and second buffers that have buffer output terminals and also have buffer input terminals coupled to differential output terminals of said differential pair;
said first and second transistors are coupled to said buffer output terminals; and
said correction sensor is coupled to differential input terminals of said differential amplifier.

23. The amplifier of claim 16, wherein:
said differential amplifier includes a differential pair of transistors and first and second buffers that have buffer output terminals and also have buffer input terminals coupled to differential output terminals of said differential pair;
said first and second transistors are coupled to said differential input terminals of said differential amplifier; and
said correction sensor is coupled to differential output terminals of said differential amplifier.

24. The amplifier of claim 16, wherein said first and second

transistors are coupled to one of upstream and downstream portions of said differential signal path and said differential correction signal is coupled to the other of said upstream and downstream portions.

25. The amplifier of claim 16, wherein said first and second transistors are directly connected to said different sides of said differential signal path.

26. An pin electronics system for testing of a device-under-test (DUT) at a DUT system port, comprising:

a pin driver that applies an excitation signal to said system port;

an active load that provides a load to said system port; and

a comparator coupled to said system port to compare a response signal of said DUT to a predetermined reference signal;

wherein at least one of said pin driver, active load and comparator includes:

a) a differential pair of transistors positioned to process a differential signal along a differential signal path;

b) first and second transistors coupled to different sides of said differential signal path; and

c) a differential error amplifier that couples a differential correction signal to said differential signal path in differential response to a differential error signal generated by like terminals of said first and second transistors;

differential-heating signal errors of said differential amplifier thereby reduced by said sensor.

27. The system of claim 26, further including a bias generator that establishes respective bias parameters for at least one set of same terminals of said first and second transistors that differ from said like terminals.

28. The system of claim 26, wherein said first and second transistors are bipolar junction transistors and said like terminals are

emitters of said bipolar junction transistors.

29. The system of claim 26, wherein said first and second transistors are metal-oxide semiconductor transistors and said like terminals are sources of said metal-oxide semiconductor transistors.

30. The system of claim 26, wherein:

said differential amplifier includes a differential pair of transistors and first and second buffers that have buffer output terminals and also have buffer input terminals coupled to differential output terminals of said differential pair;

said first and second transistors are coupled to said buffer output terminals; and

said correction sensor is coupled to said buffer input terminals.

31. The system of claim 26, wherein:

said differential amplifier includes a differential pair of transistors and first and second buffers that have buffer output terminals and also have buffer input terminals coupled to differential output terminals of said differential pair;

said first and second transistors are coupled to said buffer output terminals; and

said correction sensor is coupled to differential input terminals of said differential amplifier.

32. The system of claim 26, wherein:

said differential amplifier includes a differential pair of transistors and first and second buffers that have buffer output terminals and also have buffer input terminals coupled to differential output terminals of said differential pair;

said first and second transistors are coupled to said differential input terminals of said differential amplifier; and

said correction sensor is coupled to differential output terminals of said differential amplifier.

33. The system of claim 26, wherein said first and second

transistors are coupled to one of upstream and downstream portions of said differential signal path and said differential correction signal is coupled to the other of said upstream and downstream portions.

34. The amplifier of claim 26, wherein said first and second transistors are directly connected to said different sides of said differential signal path.